Appl. No. 10/533,141
Amdt. dated September 13, 2007
Reply to Office Action of June 13, 2007

REMARKS

Claims 1-10 are pending and have been examined. Claims 1-10 have been rejected under 35 U.S.C. §103. Claims 5 and 10 have been rejected under 35 U.S.C. §112, second paragraph. Claims 1-4 are amended. Claims 5-10 have been cancelled. Claims 1-4 remain for consideration upon entry of the present Amendment. No new matter has been added.

The Examiner objects to FIG. 1 of the drawings and requires a corrected drawing. The Examiner states that FIG. 1 should be designated as "Prior Art" because only that which is old is illustrated. A corrected drawing for FIG. 1 including the "Prior Art" designation, consistent with 37 CFR §1.121(d) is appended hereto. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the objection to the drawings.

The Examiner rejects Claims 5 and 10 under 35 U.S.C. §112, second paragraph, as allegedly lacking sufficient antecedent basis. Claims 5 and 10 have been cancelled, thus the section 112 rejection is moot. Applicant therefore requests that the Examiner reconsider and withdraw the rejection of Claims 5 and 10.

Amendments are proposed to Claims 1-4 support for which is found in the original disclosure, at least at page 10, line 29 to page 17, line 21; page 20, line 2 to page 22, line 7; and FIGS. 1-5 and 7-9. Thus no new matter is added.

Claims 1-10 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,320,422 to Koh (hereinafter "Koh") in view of U.S. patent No. 6,963,230 to Morishita (hereinafter "Morishita").

In support of the rejection of Claim 1, the Examiner alleges that Koh discloses a differential circuit having a differential element provided in a signal output circuit (302), a constant current source connected to the differential element (304), and loads respectively connected to the differential element (312 and 310); and a source follower circuit (326 or 328) that outputs a differential voltage (OUT+ and OUT-) based on voltage drops developing across the loads (308 and 306), but does not teach the rest of the claim. *Office Action at pages 3-4.* However, the Examiner alleges that FIG. 2 of Morishita teaches a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off (DRM). *Office Action at page 4.* The Examiner also alleges that Koh teaches a circuit where low voltage swing, low gain, and high bandwidth are preserved. Morishita further teaches (Col. 1 lines 50-55), the "voltage-drop

system is also characterized in that, when the down-converted voltage is set constant at a level sufficiently lower than the external power supply voltage, the constant level is maintained even in the event of variation in the external power supply voltage to allow stable operation of internal circuitry." *Office Action at page 4.* The Examiner then alleges that it would have been obvious to one of ordinary skill in the art to incorporate the control system as demonstrated in Fig. 1 and Fig. 2 of Morishita, to the circuit as shown in Koh, for the purpose of maintaining a constant level, even in the event of variation in the external power supply voltage to allow stable operation of internal circuitry." *Office Action at page 4.*

Koh is merely seen to disclose "complementary source coupled logic topology suitable for high speed low voltage differential signaling. The topology . . . contains both n-type and p-type source coupled logic. The two different types of differential pairs detect input signal from rail-to-rail and provides both n-type and p-type outputs. The complementary source followers then combine and buffer the outputs of the complementary differential pairs." *Koh at column 4, lines 29-37.* As the Examiner states, Koh does not disclose "a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off."

In addition, Morishita does not disclose, teach or suggest "a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off." For example, Morishita discloses that:

> "a main amplifier MA includes . . . a current drive transistor DRM for supplying current from external power supply node EXV to internal power supply line IVL in accordance with an output signal of comparator CMM." *Morishita at column 10, lines 16-21.* "When activation control signal ACT is inactive and internal circuit 3 shown in FIG. 1 is at a standby state, the output signals of AND circuits 1c and 1d are at an L level, and MOS transistors N5 and 1e are both off. P channel MOS transistor P9 is on, and node NDA is driven to the level of external power supply voltage ExtVcc. Comparator CMM is at an inoperative state, and current drive transistor DRM is also off. *Morishita at column 10, lines 52-59.*

Morishita's node NDA is not a load in series with the DRM. Moreover, FIG. 2 of Morishita shows no other current supply connected to the internal power supply line and shows no "loads connected in series with the differential element when the differential element is off," as recited in claim 1. For example, Morishita's P channel MOS transistors P7 and P8, in FIG. 2 are not seen to be "a current supply circuit that supplies a given current to the loads connected in series with the differential element," as recited in Claim 1. Instead, the P

channel MOS transistors P7 and P8 form "a current mirror type current supply stage for supplying current to MOS transistors N3 and N4." *Morishita at column 10, lines 30-33.* Thus Morishita's FIG. 2, does not disclose, teach or suggest a "current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off," as recited in Claim 1.

Based on the above, neither Koh nor Morishita individually disclose, teach or suggest "a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off." Since neither Koh nor Morishita individually teach or suggest "a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off," any combination of Koh and Morishita further fails to disclose, teach or suggest "a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off," as recited in amended Claim 1.

Consequently, because not all of the claim recitations of Claim 1 are taught by Koh nor Morishita, individually and in combination, Applicant's Claim 1 is necessarily non-obvious, and Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1.

In support of the rejection of Claim 2, the Examiner presents similar arguments to those summarized above for Claim 1, but alleges that the current drive transistor DRM of the FIG. 13 of Morishita, teaches a first current supply that supplies a given current to the first and second loads when the first differential element is off; and alleges that the current drive transistor DRS of FIG. 13 teaches a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off. *Office Action at page 5.* The Examiner then alleges that it would be obvious to one of ordinary skill in the art to combine Koh and Morishita, for the same reasons as stated in Claim 1. *Office Action at page 5.*

As the Examiner states, Koh does not disclose teach or suggest "a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off" or "a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off."

Regarding Morishita, arguments similar to those presented above for Claim 1 also apply to Claim 2. For example, Morishita's DRM does not disclose, teach or suggest "a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off," for the reasons presented above for Claim 2. In addition, Morishita's DRS does not disclose, teach or suggest "a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off," because Morishita states that, "similar to the main amplifier MA, the sub amplifier SA includes . . . a current drive transistor DRS." *Morishita at column 4 lines 12-15.* Moreover, "the sub amplifier carries out an operation identical to that of the main amplifier." *Morishita at column 4 lines 56-58.* Morishita fails to disclose any operational difference between the DRM and the DRS. Thus the reasons present above for Claim 1 that Morishita's DRM does not disclose, teach or suggest "a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off," apply to Claim 2. Therefore, Morishita's DRS does not disclose, teach or suggest "a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off."

Based on the above, neither Koh nor Morishita individually disclose, teach or suggest "a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off" or "a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off." Since neither Koh nor Morishita individually teach or suggest "a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off" or "a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off" any combination of Koh and Morishita further fails to disclose, teach or suggest "a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off" or "a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off," as recited in amended Claim 2.

Consequently, because not all of the claim recitations of Claim 2 are taught by Koh nor Morishita, individually and in combination, Applicant's Claim 2 is necessarily non-obvious, and Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 2.

Because Claims 3-4 depend directly from Claim 2 and because Claim 2 is asserted to be non-obvious for the reasons presented above, Claims 3-4 are necessarily non-obvious. Applicant, therefore, submits that Claims 3-4 are allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claims 3-4.

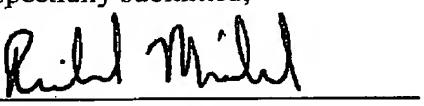
As mentioned above Claims 5-10 have been cancelled. Thus the Examiner's rejection of Claims 5-10 is moot. Applicant therefore requests that the Examiner reconsider and withdraw the rejection of Claims 5 and 10.

Applicant believes that the foregoing amendments and remarks are fully responsive to the Office Action and that the claims herein are allowable. An early action to that effect is earnestly solicited.

If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is invited to telephone the undersigned.

Applicant believes that no fees are due with the submission of this Amendment; however, if any fees are due, please charge Deposit Account No. 503342 maintained by Applicant's attorneys.

Respectfully submitted,

By 

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